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May 31, 2000

BOX PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

Re: Tominari NOMURA
TRANSMITTER WITH MEANS FOR COMPLEMENTARILY SCALING THE INPUT AND OUTPUT SIGNALS OF A D/A CONVERTER
Our Ref. Q59513

Dear Sir:

Attached hereto is the application identified above including 18 sheets of the specification, claims, 4 sheets of formal drawings, executed Assignment and PTO 1595 form, and executed Declaration and Power of Attorney.

The Government filing fee is calculated as follows:

Total claims	18	-	20	=		x	$18.00	=	$.00
Independent claims	4	-	3	=	1	x	$78.00	=	$78.00
Base Fee									$690.00
Multiple Dependent Claim Fee									$260.00
TOTAL FILING FEE									**$1028.00**
Recordation of Assignment									$40.00
TOTAL FEE									**$1068.00**

Checks for the statutory filing fee of $1028.00 and Assignment recordation fee of $40.00 are attached. You are also directed and authorized to charge or credit any difference or overpayment to Deposit Account No. 19-4880. The Commissioner is hereby authorized to charge any fees under 37 C.F.R. §§ 1.16 and 1.17 and any petitions for extension of time under 37 C.F.R. § 1.136 which may be required during the entire pendency of the application to Deposit Account No. 19-4880. A duplicate copy of this transmittal letter is attached.

Priority is claimed from June 2, 1999 based on Japanese Application No. 11-154853. The priority document is enclosed herewith.

Respectfully submitted,
SUGHRUE, MION, ZINN,
MACPEAK & SEAS, PLLC
Attorneys for Applicant

By: _____
Howard L. Bernstein
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TITLE OF THE INVENTION

"TRANSMITTER WITH MEANS FOR COMPLEMENTARILY SCALING THE INPUT AND OUTPUT SIGNALS OF A D/A CONVERTER"

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates generally to transmission systems and more specifically to a technique for improving the carrier-to-noise ratio (CNR) of radio transmissions. The present invention is particularly suitable for improving the CNR value of a code division multiple access (CDMA) transmitters such as cell-site base transmitters.

Description of the Related Art

In cell-site CDMA transmitters of a cellular mobile communication network, individual spread spectrum channel signals are synchronised and multiplexed (or digitally summed) into digital amplitude data. This amplitude data is converted by a digital-to-analog converter to an analog amplitude signal, which is up-converted, power-amplified and then transmitted. In order to prevent the digital-to-analog converter from being overloaded, the maximum amplitude of each transmit channel signal is determined in advance so that the total amplitude of the multiplexed signals corresponds to the upper limit of the digital-to-analog converter. However, the performance of the transmission system is determined by the CNR requirement of the largest signal level to be power amplified prior to modulation onto a radio frequency carrier. As a result, when not all individual channels are multiplexed during low traffic periods, the carrier-to-noise ratio of

the system becomes lower than the required value.

One approach to this problem is to use a digital-to-analog converter for each channel signal to produce a multiplex of analog amplitude signals, instead of using the single digital-to-analog converter for producing a multiplex of digital amplitude signals. However, this approach is not an economical implementation and requires additional circuitry that ensures orthogonality between any pair of analog spread spectrum channel signals.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a transmitter and a communication method for improving the carrier-to-noise ratio of a signal that has been subjected to a digital-to-analog conversion process prior to transmission.

According to a first aspect of the present invention, there is provided a transmitter comprising average power level calculation circuitry for determining the time-average power of a digital amplitude signal, and conversion circuitry for scaling the digital amplitude signal according to a first scale factor, converting the scaled digital amplitude signal to an analog amplitude signal, scaling the analog amplitude signal according to a second scale factor, and control circuitry for complementarily varying the first and second scale factors according to the time-average power.

According to a second aspect, the present invention provides a spread spectrum transmitter comprising a multiplexer for multiplexing a plurality of spread spectrum channel signals to produce a digital

amplitude signal, average power level calculation circuitry for determining the time-average power of the digital amplitude signal, and conversion circuitry for scaling the digital amplitude signal according to a first scale factor, converting the scaled digital amplitude signal to an analog amplitude signal, scaling the analog amplitude signal according to a second scale factor, and control circuitry for complementarily varying the first and second scale factors according to the time-average power.

According to a third aspect of the present invention, there is provided a communication method comprising the steps of determining the time-average power of a digital amplitude signal, scaling the digital amplitude signal according to the time-average power, converting the scaled digital amplitude signal to an analog amplitude signal, scaling the analog amplitude signal according to the time-average power complementarily to the scaling of the digital amplitude signal and transmitting the scaled analog amplitude signal.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be described in further detail with reference to the accompanying drawings, in which:

Fig. 1 is a block diagram of a CDMA transmitter according to a first embodiment of the present invention;

Fig. 2 is a timing diagram for illustrating an interpolated bit sequence;

Fig. 3 shows relationships between an N-bit sequence, an interpolated M-bit bit sequence and a selected L-bit sequence;

Fig. 4 is a block diagram of a CDMA transmitter according to a second embodiment of the present invention; and

Fig. 5 is a block diagram of a CDMA transmitter according to a third embodiment of the present invention.

DETAILED DESCRIPTION

Referring now to Fig. 1, there is shown a CDMA (code division multiple access) transmission circuit according to a first embodiment of the present invention for a communication system such as a cell-site base station of a cellular mobile communication network. It is seen in Fig. 1 that a plurality of individual digital spread spectrum channel signals (either speech or data) are multiplexed (or "digitally summed") in a multiplexer 1 into digital amplitude data. Each of the input spread spectrum signals is a signal that has been spread (scrambled) with short and long spreading codes and time-synchronized with other spread spectrum signals in a manner well known in the CDMA art.

According to this invention, the digital amplitude data from the multiplexer 1 is supplied to an interpolator 2 and an average power calculator 3 simultaneously. Average power calculator 3 calculates a time-average value of the total power level of the multiplexed amplitude data and feeds a control circuit 4.

Interpolator 2 provides interpolation on N bits of the amplitude data and produces M bits of multiplexed amplitude data, where M is greater than N. For example, if the N-bit multiplexed amplitude data has a sequence of bits $\{A_1, A_2, \ldots, A_N\}$ occurring at T-intervals, as indicated by circles in Fig. 2, the interpolator 2 calculates the amplitude

difference between successive bits and determines the gradient of a slope as $(A_i + A_{i+1})/T$ (where i = 1, 2, ... N) during each bit interval T. If one bit is interpolated between successive input bits as indicated by dots in Fig. 2, the interpolator 2 produces an M-bit output sequence in which the individual bits occur at interval T' equal to T/2.

The output of the interpolator 2 is sent to a bit shifter 5. Bit shifter selects a sequence of a predetermined number of "L" bits from bit positions of each input M-bit sequence which are specified by the control circuit 4, where the integer L is larger than N but smaller than M. As shown in Fig. 3, the bit shifter 5 may be implemented with an M-stage shift register in which default bit positions (i + 1) to (i + L) are defined. According to the average power of the multiplexed amplitude data relative to a reference power level, the control circuit 4 determines the scale factor of the input signal to the D/A converter 6 and determines the bit positions of an output L-bit sequence within an input M-bit sequence. Control circuit 4 specifies the bit positions of the output L-bit sequence and instructs the bit shifter 5 to select an L-bit sequence from the specified bit positions of the M-bit sequence.

The L-bit sequence selected by the bit shifter 5 is converted to a corresponding analog amplitude signal by a digital-to-analog converter 6. A gain-controlled amplifier 7 is connected to the output of D/A converter 6 for amplifying the analog amplitude signal according to a scale factor specified by the control circuit 4. The output of the gain-controlled amplifier 7 is modulated onto a radio frequency carrier in an up-converter 8. The modulated carrier is power-amplified by a

transmission power amplifier stage 9 and transmitted from an antenna 10.

In order to meet the carrier-to-noise ratio requirement of the transmitter at all levels of transmissions, the bit shifting of shifter 5 and the gain of amplifier 7 are complementarily controlled by the control circuit 4 in a compression-expansion mode or in an expansion-compression mode depending on the average power of the amplitude data relative to a reference power level as follows.

Control circuit 4 determines whether the calculated average power level is higher or lower than a reference (default) value which may be a maximum average power level, a minimum average power level or an intermediate value that lies anywhere between the maximum and minimum values. Assume that an intermediate value is used as the reference value. In this case, the gain-controlled amplifier 7 is initialized so that, when the average power level of the output of the multiplexer 1 is equal to the reference value, the carrier-to-noise ratio of the transmitter is controlled at the required value.

If the control circuit determines that the calculated average power is lower than the intermediate reference value, it produces a down-shift control signal that causes the bit shifter 5 to select from an interpolated M-bit sequence an L-bit sequence {(i+k+1) through (i+k+L)} that is shifted downwards by "k" bits with respect to the default bit positions as illustrated in Fig. 3, where the integer "k" represents the difference between the calculated average power and the intermediate reference power level. Then, the control circuit 4 proceeds to increment

the gain of the amplifier 7 by an integral multiple of 6 dB, i.e., 6 dB times the integer "k". Since the k-bit downward-shifted L-bit sequence is 2^k times smaller than an L-bit sequence which would be selected from the default bit positions when the calculated average power were equal to the intermediate reference value, the complementary increment of the amplifier gain by a factor 2^k controls the CNR value of the current lower-than-reference signal at the same value which would be obtained when the average power of the input signals is equal to the reference value.

If the control circuit determines that the calculated average power is higher than the intermediate reference value, it produces a down-shift control signal that causes the bit shifter 5 to select from an interpolated M-bit sequence an L-bit sequence {(i–j+1) through (i–j+L)} that is shifted upwards by "k" bits with respect to the default bit positions as illustrated in Fig. 3, where the integer "j" represents the difference between the calculated average power and the intermediate reference value. Control circuit 4 proceeds to control the amplifier 7 by decrementing its gain by an integral multiple of 6 dB, i.e., 6 dB times the integer "j". Since the j-bit upward-shifted L-bit sequence is 2^j times greater than the L-bit sequence which would be selected from the default bit positions, the complementary decrement of the amplifier gain by a factor 2^j controls the CNR value of the current higher-than-reference signal at the same value which would be obtained when the average power of the input signals is equal to the reference value.

If the multiplexed amplitude data whose calculated average

power is equal to the intermediate reference value corresponding to the default bit positions and designated as S_R, the carrier-to-noise ratio of the transmitter is given by S_R/n, where n is the background noise.

When the calculated average power of multiplexed amplitude data is 1/2 of the reference level and designated as S_L, the bit shifter 5 selects an L-bit sequence from positions one bit downward-shifted with respect to the default positions. This one-bit downward shift causes the input signal of the D/A converter 6 to be scaled up by a factor 2. Complementary to the operation of bit shifter 5, the output of the D/A converter 6 is then scaled down by a factor 2 by decrementing the gain of amplifier 7 by 6 dB. Thus, the following relation holds:

$$\{(S_L) \times (2) + n\} \times (1/2) = S_L + n/2$$

Thus, the CNR of the signal S_L is equal to $2 \times (S_L)/n$, and hence to S_R/n.

When the calculated average power of multiplexed amplitude data is two times as higher than the reference level and designated as S_H, the input of the D/A converter 6 is scaled down by a factor 2 by shifting the L-bit sequence by one bit upward with respect to the default positions. The output of the D/A converter 6 is scaled up by a factor 2 by incrementing the gain of amplifier 7 by 6 dB. Thus, the following relation holds:

$$\{(S_H) \times (1/2) + n\} \times (2) = S_H + 2n$$

Thus, the CNR of the signal S_H is equal to $(S_H)/2n$, and hence to S_R/n.

It is seen that transmissions from a CDMA cell-site base station can be maintained at a substantially constant CNR value regardless of its transmission power levels. Another feature of the present invention

is that since the average power of the multiplexed channel signals is compared with a reference power level in the control circuit 4, abnormal state of the signals can be detected. In such instances, the control circuit 4 controls the transmission power so that no interference can occur with other communication systems.

Fig. 4 shows a modified embodiment of the present invention in which a down-converter 11 and a detector 12 are connected to the output of power amplifier 9 for detecting the power level of the power amplifier 9. The output of detector 12 is used by the control circuit 8 to detect the difference between the calculated average power of the multiplexed digital amplitude data and the actual power level of the signal transmitted from the antenna 10.

Control circuit 8 controls the bit shifter 5 according to the difference between the calculated average power and the reference power level in a manner as described above. Control circuit 8 controls the gain of the amplifier 7 according to the difference between the calculated average power and the reference power level and the difference between the calculated average power and the actual power level of transmission. Thus, the gain of amplifier 7 is varied by an integral multiple of 6 dB according to the difference between the calculated average power and the reference power level in a manner as described above, plus a scale factor "α" which varies with the difference between the calculated average power and the actual transmission power level of the power amplifier 9. This feedback arrangement serves to prevent the power amplifier 9 from varying its transmission power

which would otherwise be caused by environmental conditions.

The average power of the multiplexed digital amplitude data can also be obtained by a channel management unit as shown in Fig. 5. Channel management unit 13 provides not only channel assignment and power control functions, but provides detection of the total average power of individual channel signals. Channel management unit 13 also determines spreading codes to be used by spreading circuitry 14 for scrambling the signals of assigned channels. The scrambled signals are supplied to the multiplexer 1 as the transmit spread spectrum signals mentioned above. The total average power of the transmit channel signals is supplied from the channel management unit 13 to the control circuit 4, instead of the signal calculated by the average power calculator 3 of the previous embodiments.

What is claimed is:

1. A transmitter comprising:

average power level calculation circuitry for determining the time-average power of a digital amplitude signal; and

conversion circuitry for scaling said digital amplitude signal according to a first scale factor, converting the scaled digital amplitude signal to an analog amplitude signal, and scaling the analog amplitude signal according to a second scale factor; and

control circuitry for complementarily varying said first and second scale factors according to said time-average power.

2. A transmitter as claimed in claim 1, wherein said digital amplitude signal is a multiplexed digital amplitude signal in which a plurality of digital spread spectrum signals are multiplexed.

3. A transmitter as claimed in claim 1 or 2, wherein said conversion circuitry is configured to:

compare the time-average power of said multiplexed digital amplitude signal with a reference power level and determine a differential power value; and

determine said first and second scale factors according to said differential power value.

4. A transmitter as claimed in claim 1, wherein said conversion circuitry comprises:

an interpolator for interpolating said digital amplitude signal and producing an output signal containing a greater number of bits than a number of bits contained in said digital amplitude signal;

a bit shifter for selecting a predetermined number of bits from a plurality of bit positions of said output signal of the interpolator, said plurality of bit positions being determined by said first scale factor;

a digital-to-analog converter for converting the output signal of the interpolator to an analog signal; and

a gain-controlled amplifier for amplifying the analog signal from the digital-to-analog converter at a level determined by said second scale factor.

5. A transmitter as claimed in claim 1, further comprising:

an up-converter for modulating said analog amplitude signal onto a carrier;

a power amplifier for amplifying the modulated carrier; and

detection circuitry for detecting power variation of said power amplifier,

wherein said control circuitry is responsive to the detected power variation for controlling said second scale factor.

6. A transmitter as claimed in claim 1, wherein said average power level calculation circuitry is a channel management unit.

7. A spread spectrum transmitter comprising:

a multiplexer for multiplexing a plurality of spread spectrum

channel signals to produce a digital amplitude signal;

average power level calculation circuitry for determining the time-average power of the digital amplitude signal; and

conversion circuitry for scaling said digital amplitude signal according to a first scale factor, converting the scaled digital amplitude signal to an analog amplitude signal, scaling the analog amplitude signal according to a second scale factor; and

control circuitry for complementarily varying said first and second scale factors according to said time-average power.

8. A spread spectrum transmitter as claimed in claim 7, wherein said conversion circuitry is configured to:

compare the time-average power of said multiplexed digital amplitude signal with a reference power level and determine a differential power value; and

determine said first and second scale factors according to said differential power value.

9. A spread spectrum transmitter as claimed in claim 7, wherein said conversion circuitry comprises:

an interpolator for interpolating said digital amplitude signal and producing an output signal containing a greater number of bits than a number of bits contained in said digital amplitude signal;

a bit shifter for selecting a predetermined number of bits from a plurality of bit positions of said output signal of the interpolator, said plurality of bit positions being determined by said first scale factor;

a digital-to-analog converter for converting the output signal of the interpolator to an analog signal; and

a gain-controlled amplifier for amplifying the analog signal from the digital-to-analog converter at a level determined by said second scale factor.

10. A spread spectrum transmitter as claimed in claim 7, further comprising:

an up-converter for modulating said analog amplitude signal onto a carrier;

a power amplifier for amplifying the modulated carrier; and

detection circuitry for detecting power variation of said power amplifier,

wherein said control circuitry is responsive to the detected power variation for controlling said second scale factor.

11. A transmitter as claimed in claim 7, wherein said average power level calculation circuitry is a channel management unit.

12. A communication method comprising the steps of:

a) determining the time-average power of a digital amplitude signal;

b) scaling said digital amplitude signal according to said time-average power;

c) converting the scaled digital amplitude signal to an analog amplitude signal;

d) scaling the analog amplitude signal according to said time-average power complementarily to the step (b); and

e) transmitting the scaled analog amplitude signal.

13. A communication method as claimed in claim 12, wherein the step (b) comprises the steps of:

interpolating said digital amplitude signal and producing an output signal containing a greater number of bits than a number of bits contained in said digital amplitude signal;

selecting a predetermined number of bits from a plurality of bit positions of said output signal according to said time-average power power;

converting the scaled digital amplitude signal to an analog amplitude signal; and

amplifying the analog amplitude signal according to said time-average power.

14. A communication method as claimed in claim 12, further comprising:

modulating said analog amplitude signal onto a carrier;

amplifying the modulated carrier;

detecting power variation of the modulated carrier;

controlling amplification gain of said analog amplitude signals according to the detected power variation.

15. A communication method comprising the steps of:

a) determining the time-average power of a digital amplitude signal;

b) comparing the determined time-average power with a reference power level and determining a differential power value;

c) scaling said digital amplitude signal according to said differential power value;

d) converting the scaled digital amplitude signal to an analog amplitude signal;

e) scaling the analog amplitude signal according to said differential power value complementarily to the step (c); and

f) transmitting the scaled analog amplitude signal.

16. A communication method as claimed in claim 15, wherein the step (c) comprises the steps of:

interpolating said digital amplitude signal and producing an output signal containing a greater number of bits than a number of bits contained in said digital amplitude signal;

selecting a predetermined number of bits from a plurality of bit positions of said output signal according to said differential power value;

converting the scaled digital amplitude signal to an analog amplitude signal; and

amplifying the analog amplitude signal according to said differential power value.

17. A communication method as claimed in claim 15, further

comprising:

modulating said analog amplitude signal onto a carrier;

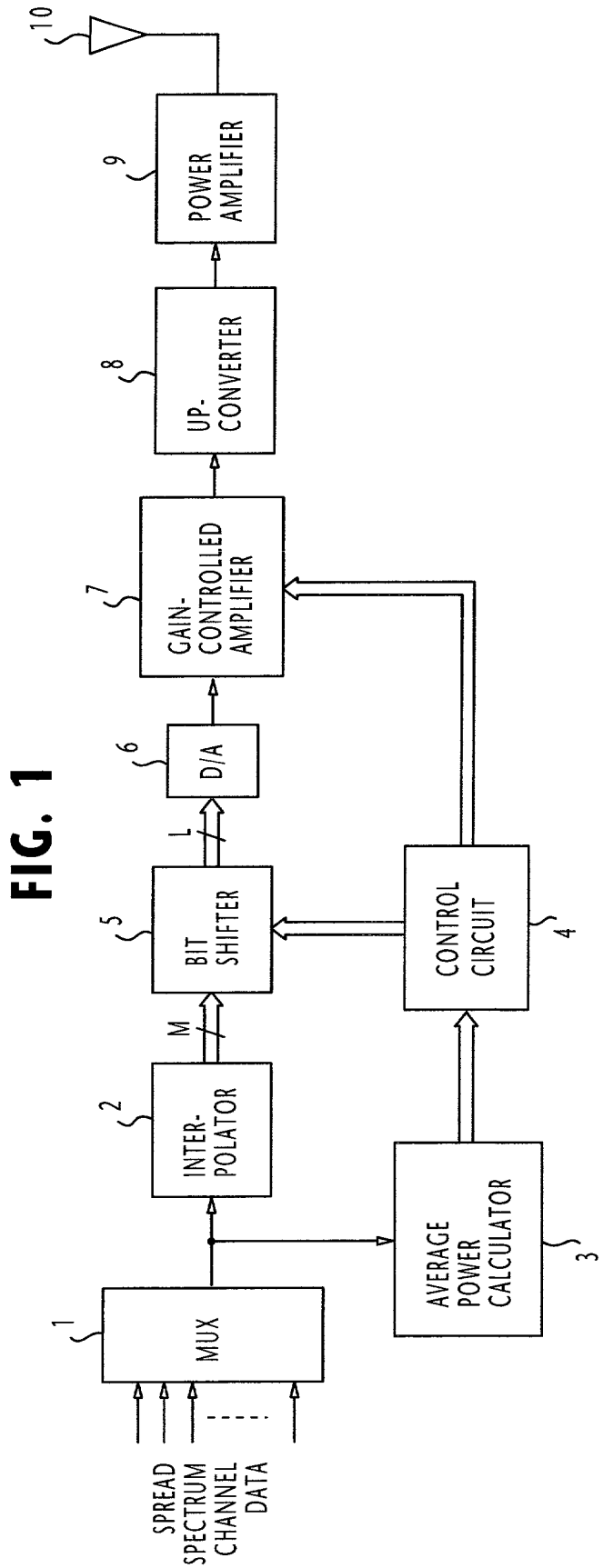
amplifying the modulated carrier;

detecting power variation of the modulated carrier; and

controlling amplification gain of said analog amplitude signals according to the detected power variation.

ABSTRACT OF THE DISCLOSURE

In a spread spectrum transmitter, a number of spread spectrum channel signals are multiplexed into a digital amplitude signal by a multiplexer (1) and the time-average power of the digital amplitude signal is determined by an average calculator (3). The digital amplitude signal is interpolated by an interpolator (2), scaled according to a first scale factor by a bit shifter (5) and converted to an analog amplitude signal by a D/A converter (6). The analog amplitude signal is then scaled by according to a second scale factor in a gain controlled amplifier (7). The first and second scale factors are complementarily varied by a control circuit (4) according to the output o the average calculator (3) so that the carrier-to-noise ratio of the transmitter is maintained substantially constant regardless of the varying power level of the multiplexed signals.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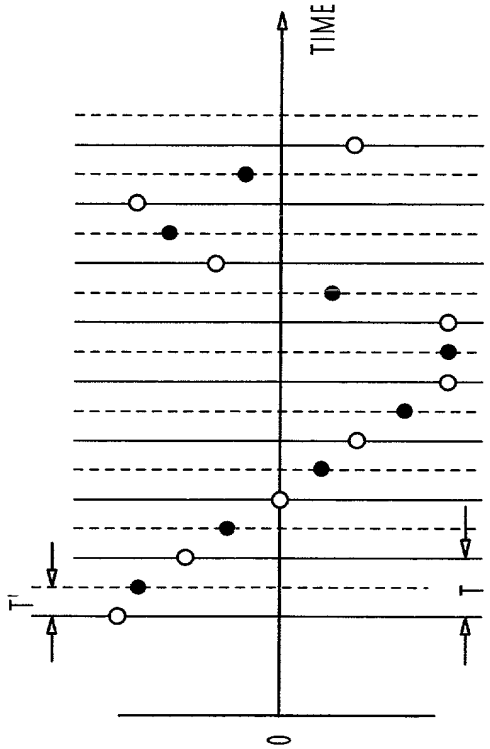
1
MUX
2
INTER-POLATOR
M
3
AVERAGE POWER CALCULATOR
4
CONTROL CIRCUIT
5
BIT SHIFTER
L
6
D/A
7
GAIN-CONTROLLED AMPLIFIER
8
UP-CONVERTER
9
POWER AMPLIFIER
10

FIG. 1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T'
T
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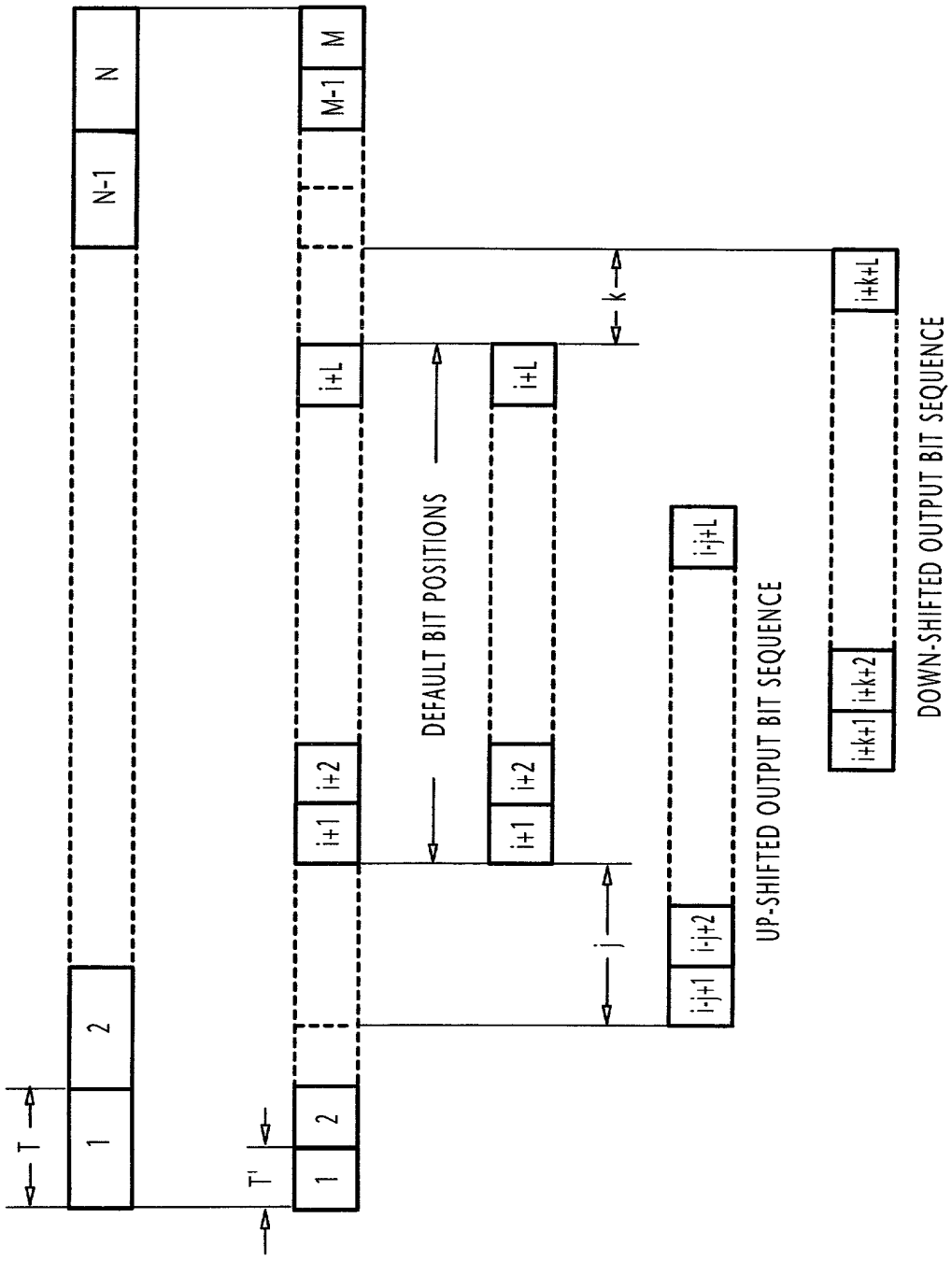
FIG. 2

FIG. 3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T'
1
2
i+1
i+2
i+L
M-1
M
DEFAULT BIT POSITIONS
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i+2
i+L
k
j
i-j+1
i-j+2
i-j+L
UP-SHIFTED OUTPUT BIT SEQUENCE
i+k+1
i+k+2
i+k+L
DOWN-SHIFTED OUTPUT BIT SEQUENCE

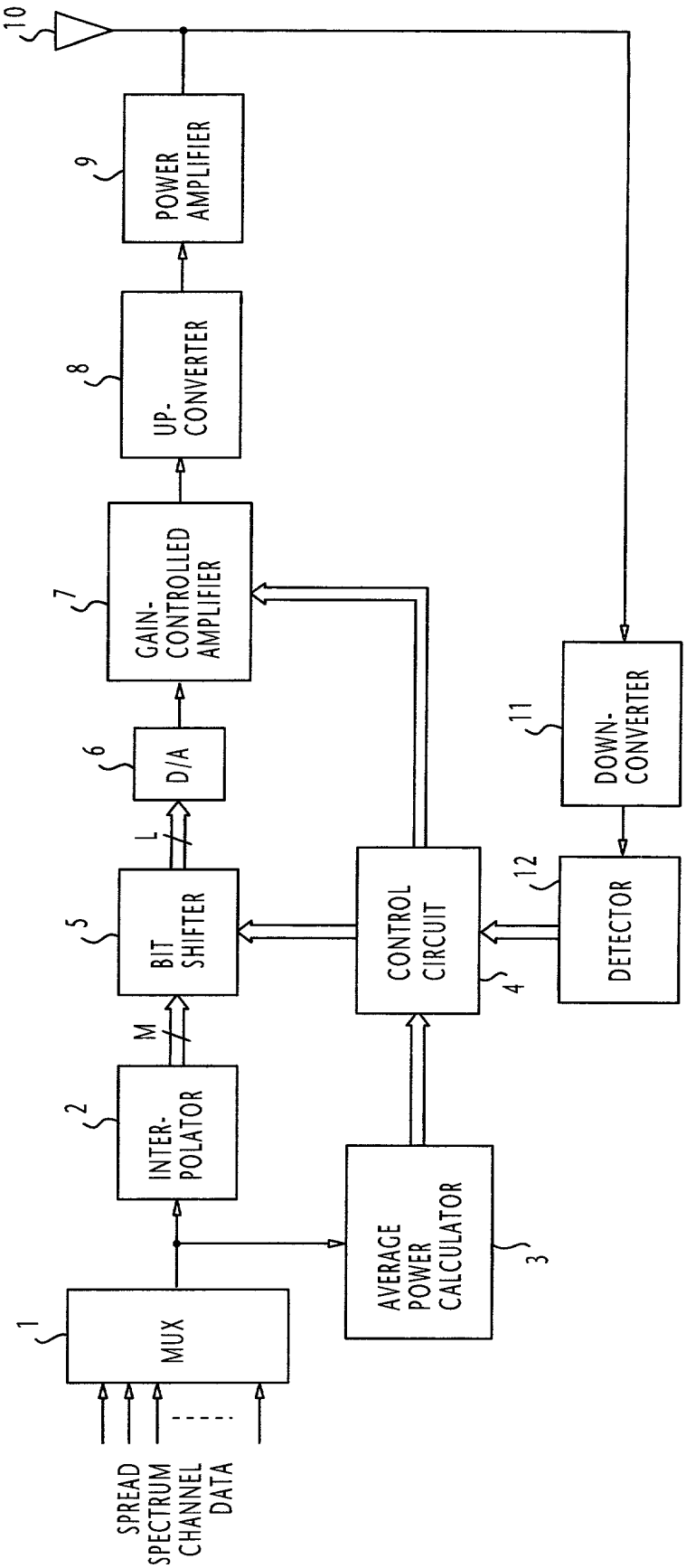
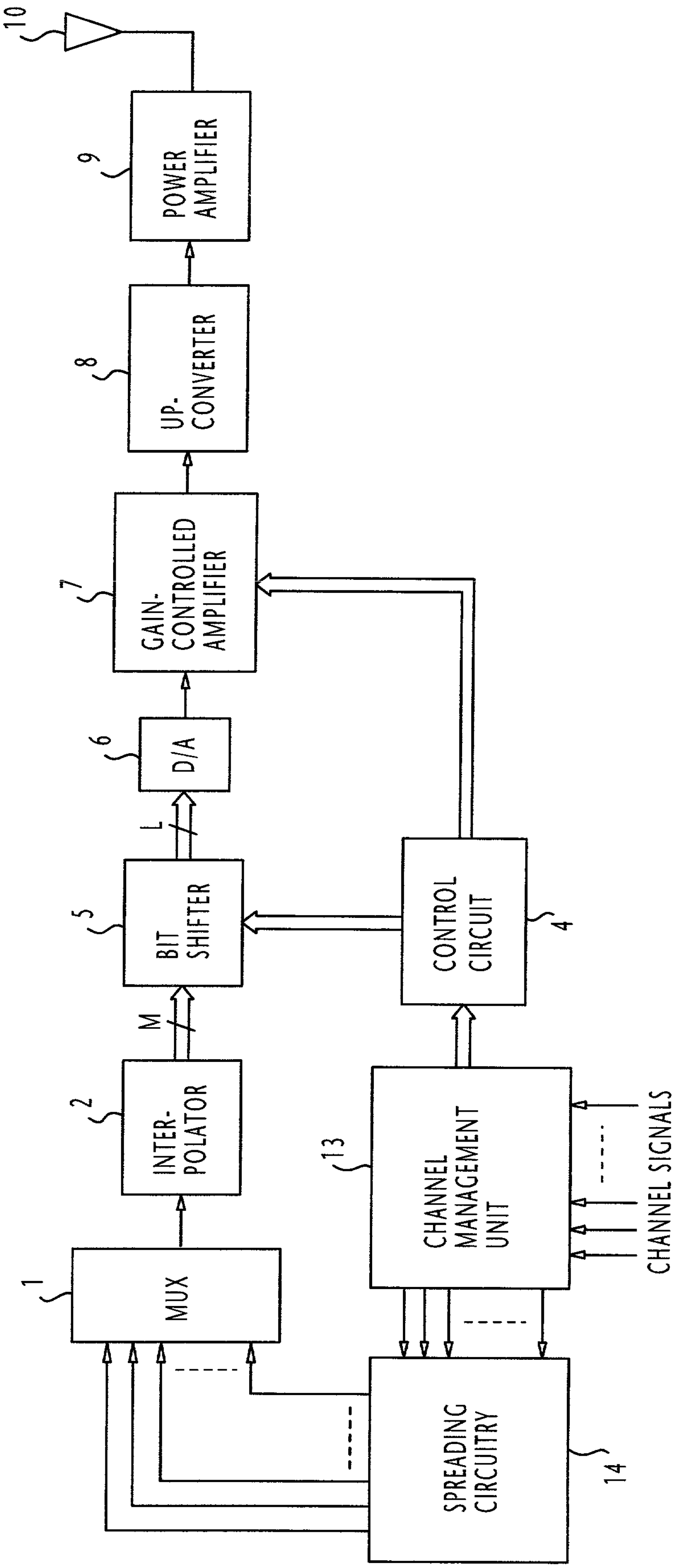

SPREAD SPECTRUM CHANNEL DATA
1
MUX
2
INTER-POLATOR
M
L
5
BIT SHIFTER
6
D/A
7
GAIN-CONTROLLED AMPLIFIER
8
UP-CONVERTER
9
POWER AMPLIFIER
10
AVERAGE POWER CALCULATOR
3
CONTROL CIRCUIT
4
11
DOWN-CONVERTER
12
DETECTOR

FIG. 4

FIG. 5


10
9
POWER
AMPLIFIER
8
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CONVERTER
7
GAIN-
CONTROLLED
AMPLIFIER
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POLATOR
1
MUX
4
CONTROL
CIRCUIT
13
CHANNEL
MANAGEMENT
UNIT
CHANNEL SIGNALS
14
SPREADING
CIRCUITRY

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アメリカ SOLE/JOINT
森崎特許事務所

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name: that I verily believe I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural names are listed below) of the subject matter claimed and for which a patent is sought in the application entitled:

TRANSMITTER WITH MEANS FOR COMPLEMENTARILY SCALING
THE INPUT AND OUTPUT SIGNALS OF A D/A CONVERTER

which application is:
_X_ the attached application
(for original application)

___ application Serial No. _____.
filed _____, and amended on
_____
(for declaration not accompanying application)

that I have reviewed and understand the contents of the specification of the above-identified application, including the claims, as amended by any amendment referred to above; that I acknowledge my duty to disclose information of which I am aware which is material to the patentability of this application under 37 C.F.R. 1.56, that I hereby claim foreign priority benefits under Title 35, United States Code §119, §172 or §365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified on said list any foreign application for patent or inventor's certificate on this invention having a filing date before that of the application on which priority is claimed:

Application Number	Country	Filing Date	Priority Claimed (yes or no)
11-154853	Japan	June 2, 1999	Yes

I hereby claim the benefit of Title 35, United States Code §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in a listed prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge my duty to disclose any information material to the patentability of this application under 37 C.F.R. 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application Serial No.	Filing Date	Status (patented, pending, abandoned)

I hereby appoint John H. Mion, Reg. No. 18,879; Donald E. Zinn, Reg. No. 19,046; Thomas J. Macpeak, Reg. No. 19,292; Robert J. Seas, Jr., Reg. No. 21,092; Darryl Mexic, Reg. No. 23,063; Robert V. Sloan, Reg. No. 22,775; Peter D. Olexy, Reg. No. 24,513; J. Frank Osha, Reg. No. 24,625; Waddell A. Biggart, Reg. No. 24,861; Robert G. McMorrow, Reg. No. 19,093; Louis Gubinsky, Reg. No. 24,835; Neil B. Siegel, Reg. No. 25,200; David J. Cushing, Reg. No. 28,703; John R. Inge, Reg. No. 26,916; Joseph J. Ruch, Jr., Reg. No. 26,577; Sheldon I. Landsman, Reg. No. 25,430; Richard C. Turner, Reg. No. 29,710; Howard L. Bernstein, Reg. No. 25,665; Alan J. Kasper, Reg. No. 25,426; Kenneth J. Burchfiel, Reg. No. 31,333; Gordon Kit, Reg. No. 30,764; Susan J. Mack, Reg. No. 30,951; Frank L. Bernstein, Reg. No. 31,484; Mark Boland, Reg. No. 32,197; William H. Mandir, Reg. No. 32,156; Scott M. Daniels, Reg. No. 32,562; Brian W. Hannon, Reg. No. 32,778 and Abraham J. Rosner, Reg. No. 33,276, my attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, and request that all correspondence about the application be addressed to SUGHRUE, MION, ZINN, MACPEAK & SEAS, 2100 Pennsylvania Avenue, N.W., Washington, D.C. 20037-3202.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date May 25, 2000

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